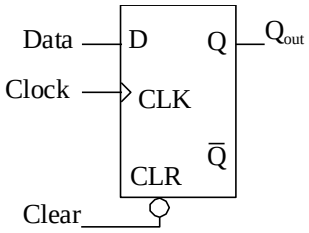
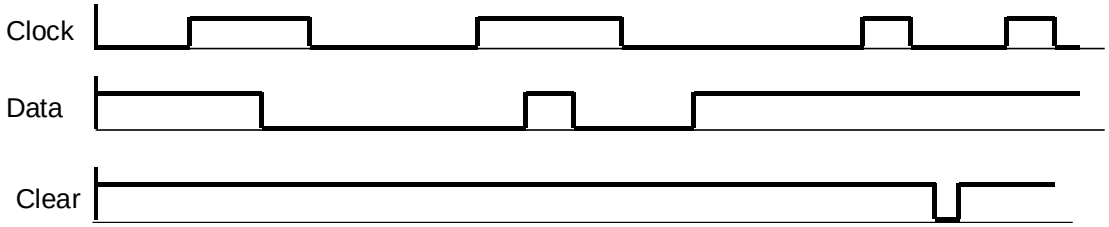
Analog & Digital Electronics

HOMEWORK ASSIGNMENT 10: **Due Monday, May 14**

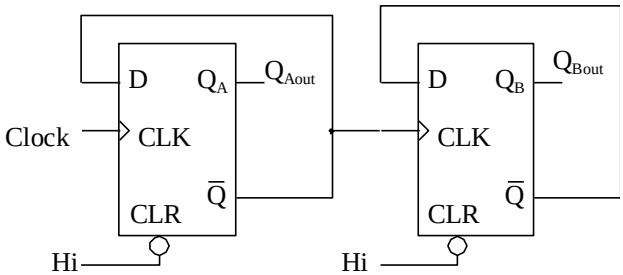
1. Make a debounce circuit out of two dual input NOR gates, an appropriate switch and resistors.

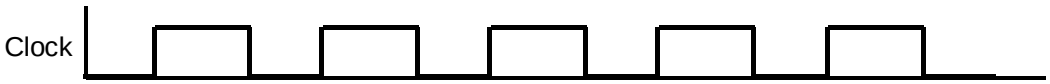
2. This tests your basic understanding of D flip flops. For the given inputs, record the output (Q) for the positive edge triggered D flip flop at the right. Note that the clear is active Low. Assume Q_{out} is initially High.





3. Draw the two outputs (Q_A & Q_B) for the two flip flops at the right. Assume the Clears and Presets are High (inactive) and the Q's are initially Low.





4. Consider the circuit at the right. The D flip-flops are positive edge triggered and have been cleared so that the Q's = 0 at the beginning. What does the Y output look like for the given input (assuming the clear and preset are HI or inactive from t=0 on)? The circuit is useful for measuring the period of a clock input. Y is used to gate another reference oscillator.